A Novel Control Strategy of Circulating Currents in Parallel Single-Phase Boost Rectifiers

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***Abstract*—In this paper, a novel circulating current control scheme of paralleled single-phase boost-type full-bridge converters is proposed. The novel circulating current control scheme doesn't require any communication between paralleled converters. Simultaneously, the proposed circulating current control scheme improves the performance of the parallel system and reduces the circulating currents which result from the parallel connection. Based on this control scheme, not only input current shaping of each converter is improved, but also current sharing among paralleled converters is achieved. Both simulation and experimental results verified the validity of the proposed circulating current control scheme.**

I. INTRODUCTION

It is well-known that converters can be paralleled to increase the power capability, reliability, efficiency, and redundancy [1]-[3], [16]. In addition, the parallel structure is suitable for modularized system design and provides more flexibility in the power-capacity-augmented system in the alternative energy applications. However, when the converters are connected in parallel directly, the circulating currents are generated automatically due to the unsynchronized operation of the paralleled converter system. Hence, the operation of paralleled converters usually requires isolation [5]-[8]. The weight, size, and cost associated with isolation transformers and/or additional power sources may cause system complexity and bulky. Those solutions are undesirable in application. Therefore, the reduction of circulating currents between paralleled converters becomes a key issue. Until to the present, several methods for reducing circulating currents have been proposed [1]-[3], [5]-[11]. When converters are paralleled directly without additional passive components to reduce size and cost, inter-phase reactors may be used to provide high zero-sequence impedance [9]-[10] to reduce circulating currents. Nevertheless, the reactors can provide reasonably high impedance only at medium and high frequencies. They cannot prevent low frequency circulating currents. Recently, ideal operation status of parallel inverters is studied [17] for reducing circulating currents using synchronization operation. In practice, the synchronized operation to make uniform modulation is difficult while some of the paralleled converters are needed to be changed or fixed for maintenance. On the other hand, the synchronized operation requires communication among each converter and increases system cost [11]-[15].

Therefore, in this paper a noel simplified PWM strategy with switch constraint method is proposed to prevent circulating currents without any communication between the paralleled converters. In order to explain this method, analysis of AC and DC circulating current loops in the paralleled converter system are first introduced. For reducing AC and DC circulating current loops, a novel simplified PWM strategy of a single-phase boost rectifier is proposed. While the novel simplified PWM strategy is utilized in the paralleled converter system, none of the DC circulating current loop existed and there only existed AC circulating current loop. Furthermore, in order to control the AC circulating current loops simultaneously between the paralleled converters, a switching constraint method is also proposed with the simplified PWM strategy to reduce AC circulating currents. Both DC and AC circulating current loops are controlled in the proposed circulating current control scheme without any communication between the paralleled converters. This not only provides more flexibility in modularized paralleled system but also reduces weight, size and cost in the parallel operation.

The remainder of this paper is organized as follows. In the Section II, analysis of DC and AC circulating current loops in the paralleled converter system is presented. In order to reduce circulating current, the simplified PWM strategy for the single-phase boost rectifier is proposed in the section III. Based on the proposed simplified PWM strategy, the switching constraint method for controlling circulating currents without any communication between the paralleled converters is proposed in the section IV. In Section V, some experimental results are given for validating the proposed theory. Finally, some conclusions are offered in Section VI.

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II. ANALYSIS OF CIRCULATING CURRENTS

For a convenient explanation of how circulating current is generated, the two paralleled single-phase boost-rectifier system is considered and shown in Fig. 1. The AC side and DC side of two boost converters are connected in parallel directly without any isolation. During un-synchronized operation of paralleled converters, there exist several undesired current paths, i.e. circulating current loops, between paralleled converters which results in additional currents, namely circulating currents, and causes current distortion and unbalanced current sharing. For instance, in the circuit architecture of Fig. 1, when active switches $\boldsymbol{T_{B1+}}$ and $\boldsymbol{T_{B2-}}$ are turned on, one can find that there exists a current loop as below.

$$Loop: V_{dc}^{+} \rightarrow T_{B1+} \rightarrow B1 \rightarrow v_s^{-} \rightarrow B2 \rightarrow T_{B2-} \rightarrow V_{dc}^{-}$$

The output voltage $\boldsymbol{V_{dc}}$ is shorted directly by the loop, which produces huge short-circuit current and causes severe damages to the paralleled converters. In order to avoid short path loop which caused by the output voltage during un-synchronized operation, an additional inductor must be placed at each phase in each converter as shown in Fig. 2 where an inductance is additionally placed between input voltage source and leg B in each converter.

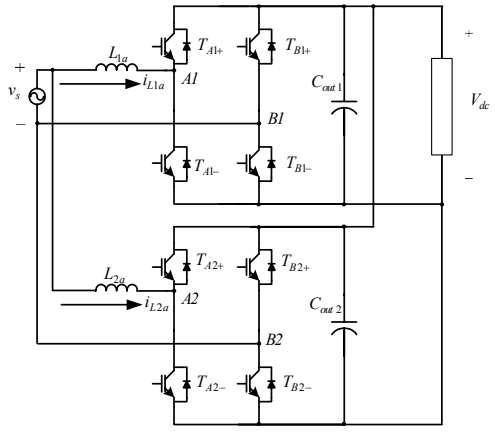


Fig.1 Two paralleled single-phase boost-rectifier converters.

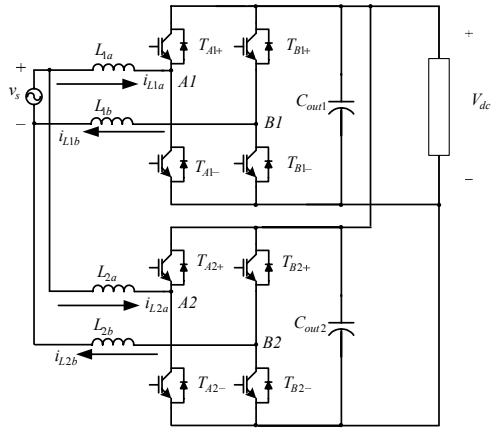


Fig.2 Two paralleled single-phase boost-rectifier converters with inductors at each phase in each converter.

Next, consider two paralleled single-phase boost-rectifier converters, shown in Fig. 2,with inductors at each phase in each converter. When the switches $\boldsymbol{T_{A1+}}$, $\boldsymbol{T_{B1+}}$, $\boldsymbol{T_{A2+}}$ and $\boldsymbol{T_{B2-}}$ are turned on, one can find that there exist two different kinds of circulating current loops, i.e. DC and AC circulating current loops. For this condition, the DC and AC circulating current loops are described as follows:

$$\boldsymbol{DC\ Loop\ 1:}\quad V_{dc}^{+} \rightarrow T_{B1+} \rightarrow B1 \rightarrow v_s^{-} \rightarrow B2 \rightarrow T_{B2-} \rightarrow V_{dc}^{-}$$

$$\boldsymbol{AC\ Loop\ 1:}\quad v_s^{+} \rightarrow A2 \rightarrow T_{A2+} \rightarrow V_{dc}^{+} \rightarrow T_{B1+} \rightarrow B1 \rightarrow v_s^{-}$$

Where DC Loop is defined as the current loop caused by the output voltage V_{dc} without passing through v_s , and AC Loop is defined as the current loop caused by the input voltage v_s without passing through $\boldsymbol{V_{dc}}$. Both DC and AC loops are the undesired loops in the paralleled converter operation system. In this paper, the proposed simplified PWM strategy combined with the switching constraint method not only eliminates the DC circulating-current loops but also control the AC circulating current loops without any communication among the paralleled converter system.

III. PROPOSED SIMPLIFIED PWM STRATEGY

First, consider a single-phase boost rectifier as shown in Fig. 3. In general, the bipolar or unipolar PWM strategies are adopted to control input current and output voltage. In order to reduce circulating current loops in the parallel system, a simplified PWM strategy is proposed. The proposed simplified PWM strategy not only reduces circulating currents but also reduces switching number so that the system performance increases and switching losses decrease. Next, in order to understand how to achieve power factor correction in the ac side and voltage regulation in the output DC side, it requires the current increasing/decreasing statuses for the input inductors. Thus, consider the input current increasing and decreasing statuses in these conditions (1) $v_s > 0$ and (2) $v_s < 0$.

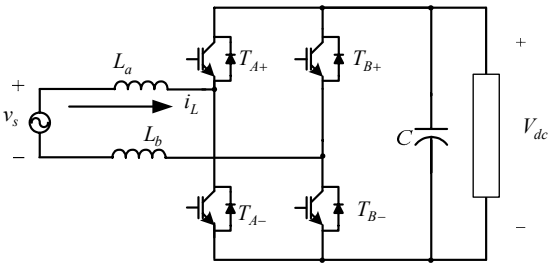
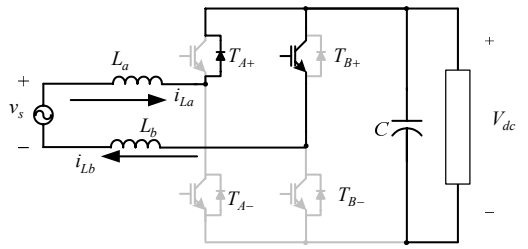


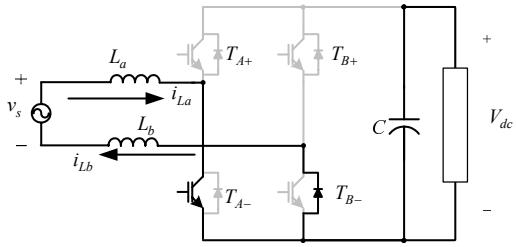
Fig.3 A single-phase boost-rectifier converter.

A. *Input voltage source* $v_s > 0$

While $v_s > 0$, the equivalent circuit under $T_{B+}\ ON$ or $T_{A-}\ ON$ increases the inductor current, and the total inductor voltage is v_s , the operation circuit of $T_{B+}\ ON$ and $T_{A-}\ ON$ are shown in Fig. 4 (a) and Fig. 4 (b), respectively.



(a)



(b)

Fig. 4 Operation circuit under (a) T_{B+} *ON* (b) T_{A-} *ON* while $v_s > 0$

Using KVL in Fig. 4(a) and (b), the voltage equation is obtained.

$$v_s - L_a \frac{d}{dt} i_L - L_b \frac{d}{dt} i_L = 0$$

Where $i_L = i_{La} = i_{Lb}$, If all the switches are OFF, the cross voltage of the both inductors is $v_s - V_{dc}$, that decreases the inductor current and the operation circuit is shown in Fig. 5.

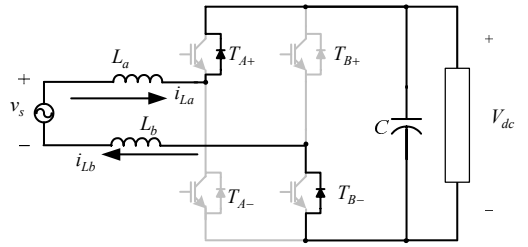


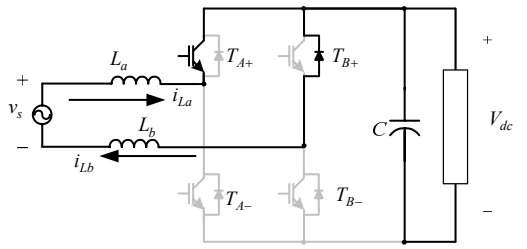
Fig. 5 Operation circuit under all the switches are OFF while $v_s > 0$

Again, using KVL in Fig. 5, the voltage relationship is described as follows.

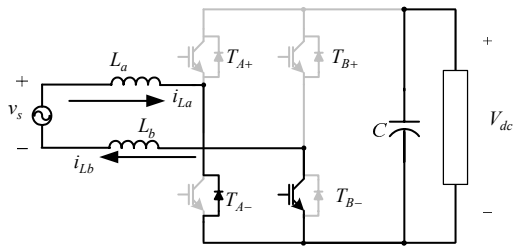
$$v_s - L_a \frac{d}{dt} i_L - V_{dc} - L_b \frac{d}{dt} i_L = 0$$

B. Input voltage source $v_s < 0$

While $v_s < 0$, the equivalent circuits under both T_{A+} *ON* and T_{B-} *ON* decrease the inductor current, and the inductor voltage across L_a and L_b is v_s, the operation circuit of T_{A+} *ON* and T_{B-} *ON* are shown in Fig. 6(a) and Fig. 6(b), respectively. The corresponding equivalent circuits under T_{A+} *ON* and T_{B-} *ON* are identical.



(a)



(b)

Fig. 6 Operation circuit under (a) T_{A+} *ON* (b) T_{B-} *ON* while $v_s < 0$

Using KVL in Fig. 6(a) and 6(b), one can obtain the voltage equation as follows.

$$v_s - L_a \frac{d}{dt} i_L - L_b \frac{d}{dt} i_L = 0$$

On the other hand, if all the switches are OFF as shown in Fig. 7, the total cross voltage of the both inductors is $v_s + V_{dc}$, that increases the inductor current.

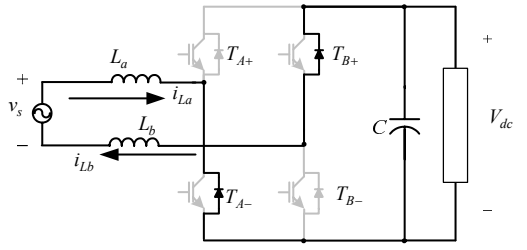


Fig. 7 Operation circuit under all the switches OFF while $v_s < 0$

Using KVL in Fig. 7, the voltage relationship is described as follows.

$$v_s - L_a \frac{d}{dt} i_L + V_{dc} - L_b \frac{d}{dt} i_L = 0$$

With the aforementioned understanding, one can summarize the circuit statuses of the boost rectifier in Table I while $v_s > 0$ and $v_s < 0$. In the condition $v_s > 0$, both status A and status B increase the inductor current and status E decreases the inductor current. The statuses A, B, E can achieve proper current shaping while $v_s > 0$. In the condition $v_s < 0$, both status C and status D decrease the inductor current and status E increases the inductor current. The statuses C, D, E also can achieve proper current shaping while $v_s < 0$.

Table 1 Switching combination of the boost rectifier

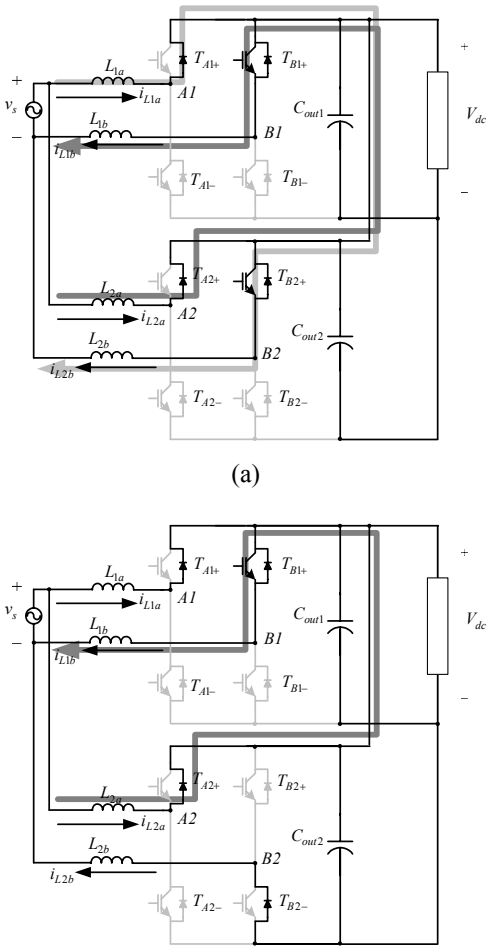
	Status	T_{A+}	T_{A-}	T_{B+}	T_{B-}	Inductor status
$v_s > 0$	A	**OFF**	**OFF**	**ON**	**OFF**	$v_{La}, v_{Lb} > 0$
	B	**OFF**	**ON**	**OFF**	**OFF**	
	E	**OFF**	**OFF**	**OFF**	**OFF**	$v_{La}, v_{Lb} < 0$
$v_s < 0$	C	**ON**	**OFF**	**OFF**	**OFF**	$v_{La}, v_{Lb} < 0$
	D	**OFF**	**OFF**	**OFF**	**ON**	
	E	**OFF**	**OFF**	**OFF**	**OFF**	$v_{La}, v_{Lb} > 0$

IV. PROPOSED SWITCHING CONSTRAINT METHOD

To achieve better current shaping and reduce the circulating currents in the parallel system, the conventional method [2] control single-phase paralleled system using two current sensors to prevent DC circulating currents. In this paper, only a current sensor is used to sensor the input current of each converter, so the switching status in Table 1 is considered to be constrained. For a convenient explanation of how to choose the switching statuses to control the circulating currents in the parallel system, first, one can consider the condition $v_s > 0$ as shown in Fig. 8. The operation status of two paralleled converters is indicated as status (x, y), where x, y represent the statuses of two converters, respectively. Fig. 8(a) is the parallel system in status (A, A) and Fig. 8(b) is the parallel system in status (A, E).

It follows from Fig. 8(a) and Fig. 8(b) that when converter 2 changes the status from A to E, the circulating current loop flows from converter 2 to converter 1(i.e. self-generated circulating current loop of converter 2) is still existed as shown in the black loop of Fig. 8(a) and Fig. 8(b). Although converter 2 can eliminate the circulating current loop generated by converter 1 as shown in the gray loop of Fig. 8(a), but converter 2 cannot eliminate the circulating current loop generated by itself. This implies that converter 2 cannot control self-generated circulating current while the status of converter 2 is changed from A to E. In this condition, the self-generated circulating current loops are uncontrollable and result in input current distortion and current unbalance in the parallel system.

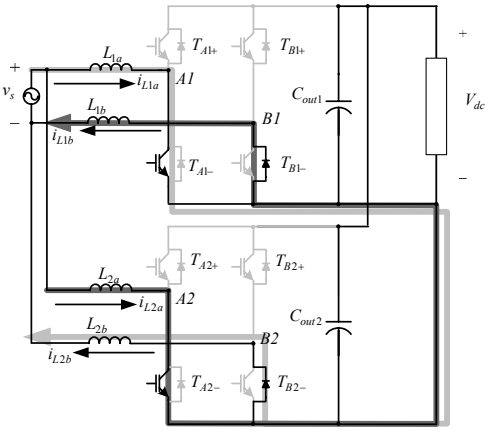
Thus, in order to control the self-generated circulating current loop, one can replace status A by B in each converter in the parallel system as shown in Fig. 9. Fig. 9(a) shows the parallel system in status (B, B) and Fig. 9(b) shows the parallel system in status (B, E). It can be observed that when converter 2 changes the status from B to E, converter 2 can eliminate the self-generated circulating current loop as shown in the black loop of Fig. 9(a). Another self-generated circulating current loop also can be easily eliminated by converter 1 while converter 1 changes status from B to E. This implies the self-generated circulating current loop in the parallel system is controllable.



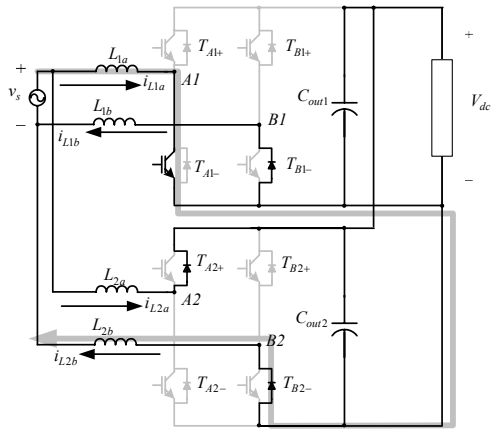
(a)

(b)

Fig. 8 Self-generated circulating current loops are uncontrollable in the parallel system while changing the system configuration from (a) status (A, A) to (b) status (A, E)



(a)



(b)

Fig. 9 Self-generated circulating current loops are controllable in the parallel system while changing the system configuration from (a) status (B,B) to (b) status (B,E)

According to the explanation above, only one current sensor is needed in each converter to avoid circulating current. In the proposed switching constraint method, the chosen statuses for parallel system can be categorized into Table 2. In the Table 2, while $v_s > 0$, status B is chosen to increase the inductor current and status E is chosen for decreasing the inductor current to achieve current shaping and voltage regulation as well as suppressing circulating current. Similarly, while $v_s < 0$, status C is chosen to decrease the inductor current and status E is chosen for increasing the inductor current to achieve current shaping and voltage regulation as well as suppressing circulating current for each converter in the parallel system.

As an illustration of two paralleled converters, the probable combination of the switching statuses is listed in Table 3. From Table 3, one can see that the circulating current loops are all AC loops and without DC loops in the proposed simplified PWM strategy. It is worth mentioned that all circulating current loops become controllable compared with using switching status in Table 1. This switching constraint concept also can be extended to N parallel single-phase converter system, if the self-generated circulating current loops are all controllable in each converter in the parallel system, then the circulating currents in the parallel system are all eliminated as well.

Table 2 Chosen statuses for parallel system in the switching constraint method

	Status	T_{A+}	T_{A-}	T_{B+}	T_{B-}	Inductor status
$v_s > 0$	B	**OFF**	**ON**	**OFF**	**OFF**	$v_{La}, v_{Lb} > 0$
	E	**OFF**	**OFF**	**OFF**	**OFF**	$v_{La}, v_{Lb} < 0$
$v_s < 0$	C	**ON**	**OFF**	**OFF**	**OFF**	$v_{La}, v_{Lb} < 0$
	E	**OFF**	**OFF**	**OFF**	**OFF**	$v_{La}, v_{Lb} > 0$

Table 3 Statuses of switching combination in the two paralleled single-phase converters in the proposed switching constraint method

No.	Parallel Status	C.C. loop	C.C. loop controllable	Switching Sync.
1	(B,B)	AC	∨	Sync.
2	(B,E)	AC	∨	Un-sync.
3	(B,C)	AC	∨	Un-sync.
4	(E,B)	AC	∨	Un-sync.
5	(E,E)	None	∨	Sync.
6	(E,C)	AC	∨	Un-sync.
7	(C,B)	AC	∨	Un-sync.
8	(C,E)	AC	∨	Un-sync.
9	(C,C)	AC	∨	Sync.

For simplicity, one can use the well-known software Power SIM to simulate the parallel converter system. As an illustration, one can consider two parallel single-phase converters as shown in Fig. 2 with the circuit parameters as listed in Table 4. It is noticed that the input voltage source is considered to be similar and closed to the actual input voltage which is operated in 60Hz frequency with 5% total harmonic distortion.

Table 4 Simulation parameters for two paralleled single-phase converters

Parameters	Converter 1	Converter 2
Switching frequency	40kHz($0°$)	40kHz($180°$)
L_{xa}	0.8210mH	0.8865mH
L_{xb}	0.8278mH	0.7860mH
Capacitor	1.4140mF	1.4140mF
Load	$150\,\Omega$	
Input voltage v_s	AC grid with $110 V_{rms}$, 60Hz fundamental frequency, with $THD_v \approx 5\%$	
Output voltage V_{dc}	300V	

The simulation results of the paralleled system without using switching constraint method are shown in Fig. 10. The input voltage v_s, input currents i_{L1a} and i_{L1b} of converter 1, input currents i_{L2a} and i_{L2b} of converter 2 are shown in Fig. 10(a), 10(b) and 10(c), respectively. One can see that $i_{L1a} \neq i_{L1b}$ and $i_{L2a} \neq i_{L2b}$, because the self-generated circulating current loops cannot be controlled by each converter in the parallel system. Fig. 11 (a) shows the leg A currents i_{L1a} and i_{L2a}, and Fig. 11 (b) shows the current difference of leg A between converter 1 and converter 2, namely $i_{L1a} - i_{L2a}$. From Fig. 10, one can find that the currents of each converter are unbalanced and distorted seriously due to the uncontrollable circulating currents. In addition, the current distribution between two paralleled converters is not equal as shown in Fig. 11.

Fig. 12 shows the simulation results of the paralleled system with proposed switching constraint method. The input voltage v_s, input currents i_{L1a} and i_{L1b} of converter 1, input currents i_{L2a} and i_{L2b} of converter 2 are shown in Fig. 12 (a),

(b) and (c), respectively. The currents of i_{L1a}, i_{L2a} and i_{L1a} - i_{L2a} are shown in Fig. 13(a) and (b), respectively. From Fig. 12, one can find that the current of each converter are balanced and have good current shape. In addition, the current distribution between two paralleled converters is improved as shown in Fig. 13.

Compared Fig. 10 (b), (c) with Fig. 12 (b), (c), one can find that the shape of the line currents have been improved and have been approached to the input voltage waveform. The circulating currents are indeed reduced in the proposed switching constraint method.

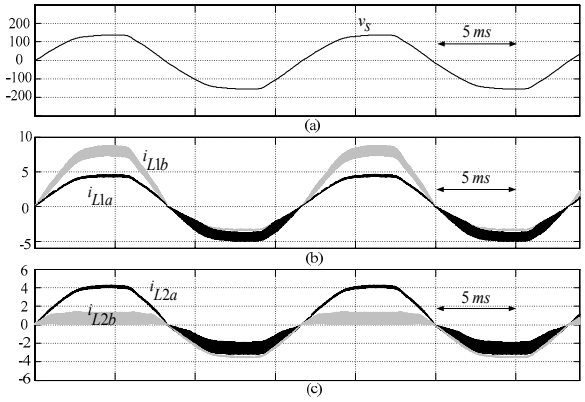


Fig. 10 Simulation Results without switching constraint method of the two paralleled converters (a) v_s (b) i_{L1a} [black] and i_{L1b} [gray] (c) i_{L2a} [black]and i_{L2b} [gray]

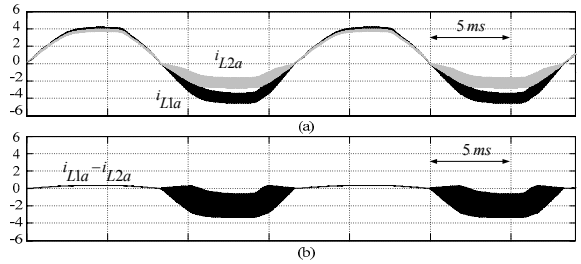


Fig. 11 Simulation Results without switching constraint method of the two paralleled converters (a) i_{L1a} [black] and i_{L2a} [gray] (b) i_{L1a} - i_{L2a}

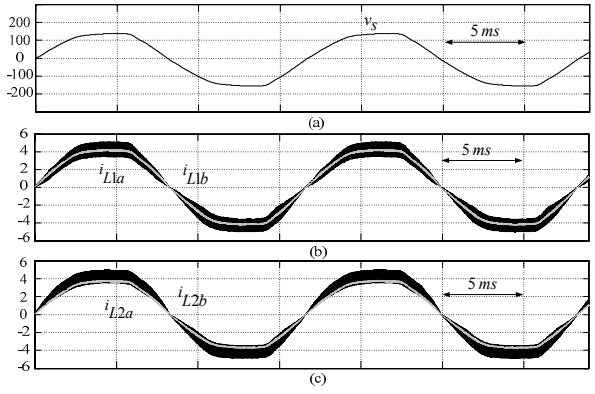


Fig. 12 Simulation Results with proposed switching constraint method of the paralleled system (a) v_s (b) i_{L1a} [black] and i_{L1b} [gray] (c) i_{L2a} [black] and i_{L2b} [gray]

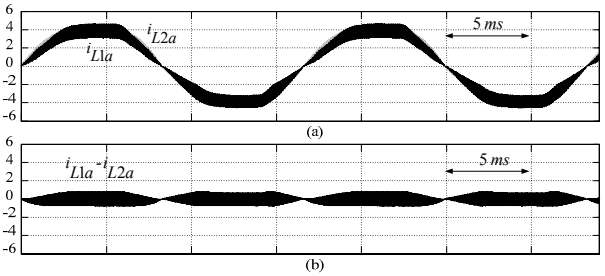


Fig. 13 Simulation Results with proposed switching constraint method of the paralleled system (a) i_{L1a} [black] and i_{L2a} [gray] (b) i_{L1a} - i_{L2a}

V. EXPERIMENTAL RESULTS

A prototype system is constructed to facilitate the validity of the proposed switching constraint method as verification. In this experiment, the adopted active switches are the Isolated-gate bipolar transistors (IXGH30G60) without body diode and the diodes (DSEP2906A) are adopted as the body diodes for active switches. The controller is implemented with a Spartan-3E XC3S250E FPGA. Consider two paralleled single-phase converters as shown in Fig. 2 with the circuit parameters which is the same as the simulation specification as listed in Table 4. It is should be noted that the actual input voltage is the 60Hz fundamental frequency with about 5% THD.

Fig. 14 and Fig. 15 show the experimental results without the proposed switching constraint method of the paralleled system. The measured input voltage v_s, input currents i_{L1a} and i_{L1b} of converter 1, input currents i_{L2a} and i_{L2b} of converter 2 are shown in Fig. 14 (a), (b) and (c), respectively. And the measured waveform line currents i_{L1a}, i_{L2a} and current difference i_{L1a} - i_{L2a} of line current in leg A are shown in Fig. 15 (a), (b), respectively. From Fig. 14, one can find that the input line currents i_{L1a}, i_{L1b}, i_{L2a} and i_{L2b} are distorted seriously without the proposed switching constraint method. From Fig. 15, it is obvious that the current distribution, due to the circulating currents, is not equal between two converters in the parallel system.

Fig. 16 and Fig. 17 show the experimental results with the proposed switching constraint method of the paralleled system. The measured input voltage v_s, input currents i_{L1a} and i_{L1b} of converter 1, input currents i_{L2a} and i_{L2b} of converter 2 are shown in Fig. 16 (a), (b) and (c), respectively. In addition, the measured input currents i_{L1a}, i_{L2a} of converter 1 and current difference i_{L1a} - i_{L2a} of line current in leg A are shown in Fig. 17 (a), (b), respectively. From Fig. 16, one can find that the input currents of each converter are balanced and indeed achieve better current shaping compared with Fig. 14. It follows from Fig. 17 that the current distribution betweens two parallel converters is improved by using the proposed switching constraint method in the parallel system.

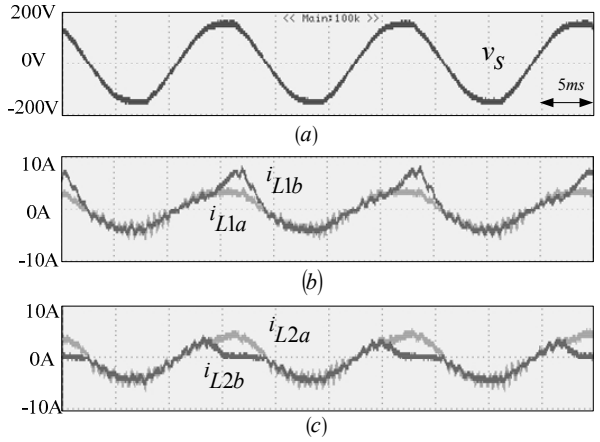


Fig. 14 Measured waveforms without proposed switching constraint method of the paralleled system (a) v_s (b) i_{L1a} [gray] and i_{L1b} [black] (c) i_{L2a} [gray] and i_{L2b} [black].

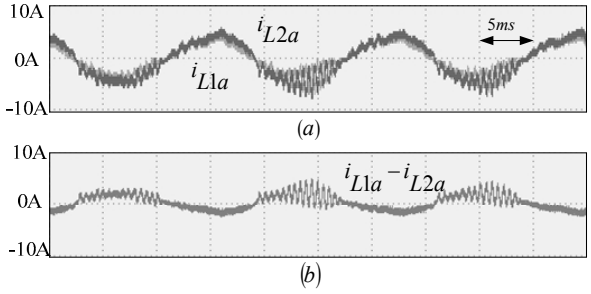


Fig. 15 Measured waveforms without proposed switching constraint method of the paralleled system (a) i_{L1a} [gray] and i_{L2a} [black] (b) i_{L1a} - i_{L2a}

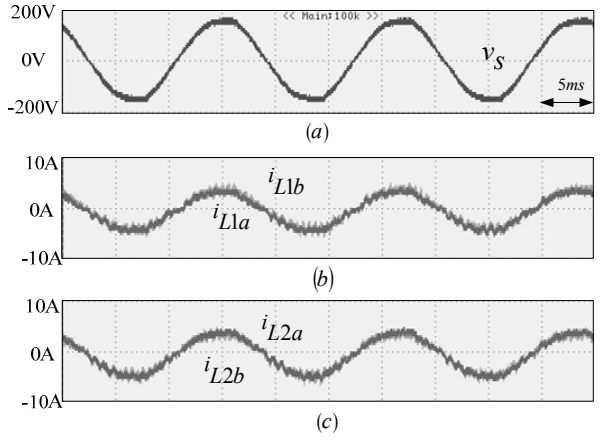


Fig. 16 Measured waveforms with proposed switching constraint method of the paralleled system (a) v_s (b) i_{L1a} [gray] and i_{L1b} [black] (c) i_{L2a} [gray] and i_{L2b} [black].

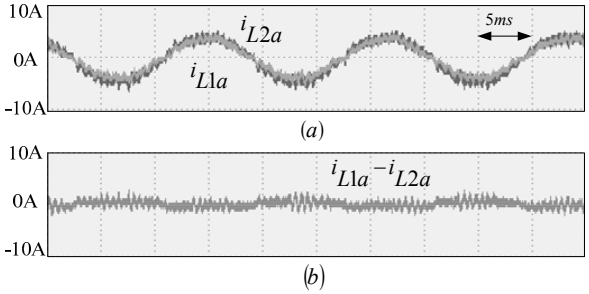


Fig. 17 Measured waveforms with proposed switching constraint method of the parallel system (a) i_{L1a} [gray] and i_{L2a} [black] (b) i_{L1a} - i_{L2a}

VI. CONCLUSION

In this paper, a switching constraint method is proposed to reduce the circulating currents without any communication among the paralleled converters in the parallel system. Some simulation results are given to verify the validity of the proposed switching constraint method. In addition, a prototype system is constructed to facilitate the theoretical results as verification. From simulation and experimental results, the proposed control scheme can indeed reduce the circulating currents in the parallel system. Therefore, the shape of the input line currents is controlled in sinusoidal waveform and in phase with the input voltage.

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